DECISION FEEDBACK EQUALIZER
WITH DYNAMIC FEEDBACK CONTROL

RELATED APPLICATIONS

This is a continuation-in-part of U.S. patent application no. 10/322,024, filed December 17, 2002.

BACKGROUND OF THE INVENTION

1.   Field of the Invention

The present invention relates to signal transmission and detection, and in particular, to techniques for compensating for signal distortions caused by signal dispersion and nonlinearities within the signal transmission media.

2.   Description of the Related Art

Signal processing architectures for intersymbol interference (ISI) equalization as used for communications transmission and/or storage systems may be divided into two categories: discrete-time architecture and continuous-time architecture. Discrete-time architectures, commonly used in current systems, use a sampled approach to render the input continuous-time, analog waveform in discrete form. Typically, a high resolution A/D converter, which follows the analog anti-aliasing filter, is used as the sampler at the analog front end. Continuous-time architectures use an analog continuous-time approach which directly processes and equalizes the incoming analog waveform while remaining in the continuous time domain until the final data bit stream is generated.

At present, those signal processing architectures having a feedforward transversal filter and a feedback filter as their basic components are considered, and in particular, the following scenarios: discrete-time/continuous-time architectures with fractionally-spaced (i.e., tap spacing less than symbol-spaced) feedforward taps; continuous-time architecture with feedback that is nominally symbol-spaced; continuous-time/discrete-time architectures with fractionally-spaced feedback. For purposes of the presently claimed invention, the following discussion concerns "fat tap" adaptation to cover the continuous-time architecture with fractionally-spaced

feedback; however, such discussion may be readily extended to cover the other scenarios as well.

Fractional-spaced feedforward filters have commonly been used either as stand-alone linear equalizers or in combination with Decision Feedback. Advantages

5   of fractional-spaced versus symbol-spaced feedforward filters include: added robustness to constant or slowly varying sampling phase offset or sampling jitter; and improved signal-to-noise ratio (SNR) sensitivity, particularly in the absence of complete channel information, due to the role of the fractional-spaced filter as a combined adaptive matched filter and equalizer.

10   The adaptation technique for the tap coefficients have always implicitly assumed independence in the adaptation of the successive tap coefficients, which has been based on minimizing the mean squared error (MSE) as computed using the difference between the slicer input and output. This adaptation technique is referred to as LMSE (least mean squared error) or MMSE (minimized mean squared error)

15   adaptation. It can be shown that the LMSE adaptation for both fractional feedforward or symbol spaced feedback at iteration $k+1$ reduces to the following coefficient update equations:

$$\underline{c}^{(k+1)} = \underline{c}^{(k)} + \mu e^{(k)} \underline{s} \quad \text{(discrete-time adaptation case)}$$

where $\underline{c}^{(k)}$ is the tap coefficient vector and $e^{(k)}$ the corresponding error at the

20   k^{th} iteration, $\underline{s}$ is the vector with components as the input waveform to the corresponding tap mixer and μ is a constant and is an adaptation parameter; and

$$\underline{c} = \int_0^t \mu \cdot e(t) \underline{s}(t) dt \quad \text{(continuous-time adaptation case)}$$

with similar terminology as above.

When continuous-time feedback is considered, a number of difficulties are

25   encountered. For example, it is difficult and sometimes unfeasible to design precisely symbol-spaced, flat group delay filters. If the total group delay on the feedback path for canceling successive past symbols is even slightly different from the corresponding symbol period, the performance loss can be substantial. This may necessitate the need for using fractionally-spaced feedback filters. Fractionally-spaced

30   feedback filters may also be needed to account for the slicer-induced jitter and/or the data bits pattern-specific group delays due to frequency dependent group delays of the slicer, mixer and any other analog/digital component on the feedback data path.

Further when an equalizer with fractionally-spaced feedback taps is used, independent LMS adaptation of the successive feedback taps fails because of the strongly correlated nature of the fractional tap-spaced feedback data.

5   SUMMARY OF THE INVENTION

A decision feedback equalizer with dynamic feedback control for use in an adaptive signal equalizer in accordance with the presently claimed invention includes timing within the decision feedback loop that is dynamically controlled to optimize

10   recovery of the data signal by the output signal slicer.

In accordance with one embodiment of the presently claimed invention, a decision feedback equalizer with dynamic feedback control for adaptively controlling a pre-slicer data signal that is sliced to provide a post-slicer data signal includes signal combining circuitry, signal slicing circuitry, decision feedback circuitry and signal

15   differentiation circuitry. First signal combining circuitry combines a feedback signal and an input signal representing a plurality of data to provide a pre-slicer signal. The signal slicing circuitry is coupled to the first signal combining circuitry and slices the pre-slicer signal to produce a post-slicer signal indicative of the plurality of data. The decision feedback circuitry includes input signal timing control, is coupled to the

20   signal slicing circuitry, and feeds back the post-slicer signal in response to a control signal to produce the feedback signal. Second signal combining circuitry is coupled to the signal slicing circuitry and combines the pre-slicer and post-slicer signals to produce a difference signal indicative of a difference between the pre-slicer and post-slicer signals. The signal differentiation circuitry includes a selected signal delay and

25   differentiates and delays the input signal to produce a resultant signal, wherein respective portions of the differentiated signal are delayed relative to corresponding portions of the input signal by the selected signal delay. Third signal combining circuitry is coupled to the second signal combining circuitry and the signal differentiation circuitry, and combines the difference signal and the resultant signal to

30   produce the control signal, wherein the selected signal delay is selected such that the control signal has a substantially zero AC signal component.

In accordance with another embodiment of the presently claimed invention, a decision feedback equalizer with dynamic feedback control for adaptively controlling a pre-slicer data signal that is sliced to provide a post-slicer data signal includes signal

combiner means, signal slicer means, decision feedback means and signal
differentiator means. First signal combiner means is for combining a feedback signal
and an input signal representing a plurality of data and generating a pre-slicer signal.
The signal slicer means is for slicing the pre-slicer signal and generating a post-slicer

5   signal indicative of the plurality of data. The decision feedback means is for
controlling signal timing by feeding back the post-slicer signal in response to a
control signal and generating the feedback signal. Second signal combiner means is
for combining the pre-slicer and post-slicer signals and generating a difference signal
indicative of a difference between the pre-slicer and post-slicer signals. The signal

10   differentiator means includes a selected signal delay and is for differentiating and
delaying the input signal and generating a resultant signal, wherein respective portions
of the differentiated signal are delayed relative to corresponding portions of the input
signal by the selected signal delay. Third signal combiner means is for combining the
difference signal and the resultant signal and generating the control signal, wherein

15   the selected signal delay is selected such that the control signal has a substantially
zero AC signal component.

In accordance with another embodiment of the presently claimed invention, a
method for providing decision feedback equalization with dynamic feedback control
for adaptively controlling a pre-slicer data signal that is sliced to provide a post-slicer

20   data signal includes:

combining a feedback signal and an input signal representing a plurality of
data and generating a pre-slicer signal;

slicing the pre-slicer signal and generating a post-slicer signal indicative of the
plurality of data;

25   feeding back the post-slicer signal with controlled signal timing in response to
a control signal and generating the feedback signal;

combining the pre-slicer and post-slicer signals and generating a difference
signal indicative of a difference between the pre-slicer and post-slicer signals;

differentiating and delaying the input signal and generating a resultant signal,

30   wherein respective portions of the differentiated signal are delayed relative to
corresponding portions of the input signal by a selected signal delay; and

combining the difference signal and the resultant signal and generating the
control signal, wherein the selected signal delay is selected such that the control signal
has a substantially zero AC signal component.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of decision feedback equalization (DFE) circuitry

5   in which an adaptive coefficient signal generator in accordance with the presently

claimed invention can advantageously provide for improved data signal equalization.

Figure 2 is a block diagram of the feedback portion of a DFE circuit in which

an adaptive coefficient signal generator in accordance with the presently claimed

invention is used to provide the adaptive coefficient signals.

10   Figure 3 is a block diagram of one embodiment of an adaptive coefficient

signal generator in accordance with the presently claimed invention.

Figure 4 is a block diagram of an exemplary implementation of the adaptive

coefficient signal generator of Figure 3.

Figure 5 is a block diagram of another embodiment of an adaptive coefficient

15   signal generator in accordance with the presently claimed invention.

Figure 6 is a block diagram of an exemplary implementation of the adaptive

coefficient signal generator of Figure 5.

Figure 7 is a block diagram of an alternative implementation of the adaptive

coefficient signal generator of Figure 4.

20   Figure 8 is a block diagram of an alternative implementation of the adaptive

coefficient signal generator of Figure 6.

Figure 9 is a block diagram depicting signal adaptation using correlated taps in

accordance with another embodiment of the presently claimed invention.

Figure 10 is a block diagram of another embodiment of an adaptive coefficient

25   signal generator in accordance with the presently claimed invention.

Figure 11 is a block diagram of feedforward equalization (FFE) circuitry with

which the adaptive coefficient signal generator of Figure 10 can share adaptive filter

coefficient signals.

Figure 12 is a block diagram of an exemplary implementation of an adaptive

30   filter coefficient signal generator for providing adaptive filter coefficient signals for

the adaptive coefficient signal generator of Figure 10.

Figure 13 is a block diagram of an exemplary implementation of a portion of

the adaptive coefficient signal generator of Figure 10.

Figure 14 is a block diagram of an alternative implementation of a portion of the adaptive coefficient signal generator of Figure 10.

Figure 15 is a block diagram of an exemplary implementation of the adaptive coefficient signal generator of Figure 10.

5   Figures 16A and 16B illustrate expected performance improvement with use of an analog continuous-time feedforward filter in conjunction with "fat tap" adaptation in accordance with the presently claimed invention.

Figure 17 is a block diagram of one example of an implementation of decision feedback equalization (DFE) circuitry providing improved data signal equalization in
10   accordance with another embodiment of the presently claimed invention.

Figure 18 is a block diagram of one example of an implementation of decision feedback equalization (DFE) circuitry providing improved data signal equalization in accordance with another embodiment of the presently claimed invention.

15   DETAILED DESCRIPTION

The following detailed description is of example embodiments of the presently claimed invention with references to the accompanying drawings. Such description is intended to be illustrative and not limiting with respect to the scope of the present
20   invention. Such embodiments are described in sufficient detail to enable one of ordinary skill in the art to practice the subject invention, and it will be understood that other embodiments may be practiced with some variations without departing from the spirit or scope of the subject invention.

Throughout the present disclosure, absent a clear indication to the contrary
25   from the context, it will be understood that individual circuit elements as described may be singular or plural in number. For example, the terms "circuit" and "circuitry" may include either a single component or a plurality of components, which are either active and/or passive and are connected or otherwise coupled together to provide the described function. Additionally, the term "signal" may refer to one or more currents,
30   one or more voltages, or a data signal. Within the drawings, like or related elements will have like or related alpha, numeric or alphanumeric designators. Further, while the present invention has been discussed in the context of implementations using discrete electronic circuitry (preferably in the form of one or more integrated circuit chips), the functions of any part of such circuitry may alternatively be implemented

using one or more appropriately programmed processors, depending upon the signal frequencies or data rates to be processed.

The subject matter discussed herein, including the presently claimed invention, is compatible and suitable for use with the subject matter disclosed in the

5   following copending, commonly assigned patent applications (the disclosures of which are incorporated herein by reference): U.S. patent application 10/117,293, filed April 5, 2002, and entitled "Compensation Circuit For Reducing Intersymbol Interference Products Caused By Signal Transmission Via Dispersive Media"; U.S. patent application 10/179,689, filed June 24, 2002, and entitled "Crosstalk

10   Compensation Engine For Reducing Signal Crosstalk Effects Within A Data Signal"; U.S. patent application 10/244,500, filed September 16, 2002, and entitled "Compensation Method For Reducing Intersymbol Interference Products Caused By Signal Transmission Via Dispersive Media"; U.S. patent application 10/290,674, filed November 8, 2002, and entitled "Compensation Circuit And Method For Reducing

15   Intersymbol Interference Products Caused By Signal Transmission Via Dispersive Media"; U.S. patent application 10/290,993, filed November 8, 2002, and entitled "Adaptive Signal Equalizer With Adaptive Error Timing And Precursor/Postcursor Configuration Control"; U.S. patent application 10/___,___, filed _____,____, 2002 [atty. docket S1471.00009], and entitled "Adaptive Signal Latency Control For

20   Communications Systems Signals"; U.S. patent application 10/___,___, filed _____, ____, 2002 [atty. docket S1471.00011], and entitled "Adaptive Signal Equalizer With Adaptive Error Timing And Precursor/Postcursor Configuration Control"; and U.S. patent application 10/179,996, filed June, 24, 2002, and entitled "Programmable Decoding of Codes of Varying Error-Correction Capability".

25   In accordance with the presently claimed invention, a group of two or more adjacent fractionally-spaced feedback taps are viewed to be correlated and corresponding to essentially the same symbol so that this group of fractionally-spaced taps essentially emulates a symbol-spaced feedback tap. Such a group of fractionally-spaced taps that emulates a symbol-spaced feedback tap is referred herein as a "fat

30   tap." Thus, successive fat taps emulate different symbol-spaced feedback taps. The adaptation of the taps within the fat tap should have some kind of adaptive timing interpolation between them so that the effective timing of the fat tap corresponds to the corresponding symbol timing. Further, both taps in the fat tap need to adapt together using LMSE adaptation, for instance, since their inputs are correlated.

The emphasized case will be that in which successive fat taps consist of disjoint taps and, thus, represent independent symbols (e.g., referred to as Independent Fat Tap Adaptation (IFTA)). Also emphasized will be the case with the constraint of only two taps within the fat tap.

5   Let the feedback tap spacing be denoted by τ which is sufficiently less than the symbol period. It is assumed that the feedback symbol waveform is approximately piece-wise linear within the span of time interval τ. Thus, if the feedback signal is denoted as $s(t)$, the parametric equation of the line passing through $s(t)$ and $s(t - \tau)$ may be denoted via:

10                    $$r \cdot s(t) + (1 - r) \cdot s(t - \tau)$$

for the parameter r (in general, $-\infty < r < \infty$). With the piecewise linear assumption of $s(t)$, we have:

$$s(t - \tau_r) \approx r \cdot s(t) + (1 - r) \cdot s(t - \tau)$$

for a suitable choice of the delay τ_r. Note that with the piecewise linear

15   approximation:

$$\tau_r \approx (1 - r) \cdot \tau.$$

With a linear approximation of the feedback signal waveform, we represent the two tap coefficients of the fat tap as $c \cdot r$ and $c \cdot (1 - r)$ where the quantity r is the

20   timing interpolation parameter which ideally should achieve effective symbol spaced timing for the fat tap, and the quantity c is used for LMSE adaptation for estimating the past ISI that needs to be cancelled. Thus, with these two parameters, the fat tap tries to emulate the corresponding symbol-spaced feedback tap with LMS tap coefficient c. The correlation ratio between the two adapting taps of the fat tap is then

25    $\dfrac{r}{1-r}$. It is then required to adapt the parameters c and r for the fat tap.

For the continuous-time case, the LMSE adaptation of the parameters c and r can then be shown to be:

$$c(t) = \mu_c \cdot \int_0^t e(v) \cdot [r \cdot s(v) + (1 - r) \cdot s(v - \tau)]dv ;$$

$$r(t) = \mu_r \cdot \int_0^t c(v) \cdot e(v) \cdot [s(v) - s(v - \tau)]dv$$

If, as may be typical, $sign(c) = -1$, and since $s(v) - s(v - \tau) \approx k\dfrac{d}{dt}s(v - \tau_r)$, for a

constant k, the update equation for $r(t)$ may also be simplified to:

$$r(t) = -\mu_r^1 \cdot \int_0^t e(v) \cdot \frac{d}{dv}s(v - \tau_r)dv .$$

Note that $\dfrac{d}{dt}s(t - \tau_r)$ may easily be implemented by passing the output of the fat tap

5   through a C-R differentiator block, which is a high-pass filter.

For the discrete-time case, the LMSE adaptation of the parameters c and r can

then be shown to be:

$$c^{(k+1)} = c^{(k)} + \mu_c \cdot e^{(k)} \cdot [r^{(k)} \cdot s(t) + (1 - r^{(k)}) \cdot s(t - \tau)]$$

$$r^{(k+1)} = r^{(k)} + \mu_r \cdot c^{(k)} \cdot e^{(k)} \cdot [s(t) - s(t - \tau)]$$

10   The update equation for r can also be simplified to (if its known that $sign(c) = -1$):

$$r^{(k+1)} = r^{(k)} - \mu_r \cdot e^{(k)} \cdot [s(t) - s(t - \tau)]$$

The next step is determining which pair of two (or more) taps belong to the

same fat tap. The specific two adjacent taps which form a fat tap corresponding to a

15   specific past symbol may vary depending on the group delay variations of different

analog or digital components within the feedback path such as the slicer, delay

elements, summer, mixer, etc. One approach is to hypothesize that different (disjoint)

pairs of taps correspond to different fat taps corresponding to different past symbols.

Then, depending on the values of the feedback tap coefficients after convergence,

20   specifically the timing interpolation parameter which should ideally be within the

range (0,1) and/or the hypothesis which corresponds to the minimum mean squared

error, the winning hypothesis may be selected as part of the start-up procedures of the

circuit. (As noted above, ideally $0 < r < 1$, although in general, $-\infty < r < \infty$. However,

it should be understood that maximum advantages of timing interpolation as provided

25   by the presently claimed invention are realized when $0 < r < 1$ (e.g., where the

complement $1-r$ of r when $r=0.2$ is $1-r = 1-0.2 = 0.8$). When r lies outside of the

range (0,1), i.e., $-\infty < r < 0$ or $1 < r < \infty$ (e.g., where the complement $1-r$ of r when

$r=1.2$ is $1-r = 1-1.2 = -0.2$), extrapolation takes place instead of interpolation and

performance degradation may result.

Referring to Figure 1, a decision feedback equalizer (DFE) 100 typically includes a feed forward filter 102 and a feedback filter 104. The feedback filter 104 processes the decisions d_k from the output of the final signal slicer 106. The coefficients, or gains, F^*_i can be adjusted to cancel ISI on the current symbol based upon past detected symbols. The feed forward filter 102 has N_1+N_2+1 taps while the feedback filter 104 has N_3 taps, and the output $\hat{d}_k$ 109 of the final signal summer 108 can be expressed as follows:

$$\hat{d}_k = \sum_{n=-N_1}^{N_2} c^*_n y_{k-n} + \sum_{i=1}^{N_3} F_i d_{k-i}$$

where

$c^*_n =$ tap gains for feed forward filter 102

$y_n =$ input signals to feed forward filter 102

$F^*_i =$ tap gains for feedback filter 104

$d_i (i < k) =$ previous decision made upon detected signal d_k

Accordingly, once the output d_k is provided by the output summer 108 of the feed forward filter 102, the final output d_k is decided. Then, the final output d_k and the previous decisions d_{k-1}, d_{k-2}, ... are fed back through the feedback filter 104, thereby providing the solution for the next decision $\hat{d}_{k+1}$ at the output 109 of the final signal summer 108 in the feed forward filter 102 in accordance with the foregoing equation.

More specifically, with respect to the feedback filter section 104, the output signal 107 is successively delayed through a sequence of time delay elements 110a, 110b, ... 110n (e.g., with each successive time delay element 110 imparting a time delay equal to one symbol). Each of the successively time-delayed signals 111a, 111b, ... 111n are processed in their respective adaptive gain stages 112a, 112b, ... 112n to provide corresponding adaptive feedback signals 113a, 113b, ... 113n which are summed together in a signal summing circuit 114 to produce the equalization feedback signal 115.

The adaptive gain stages 112a, 112b, ... 112n process their respective time-delayed signals 111a, 111b ... 111n based upon an error signal 117 representing the error, if any, between the post-slicer data signal 107 and the pre-slicer data signal 109. This error signal 117 is typically generated by subtracting the pre-slicer data signal 109 from the post-slicer data signal 107 in a signal summing circuit 116.

Referring to Figure 2, a feedback filter 104a for use in a DFE in a continuous time signal application includes the time delay elements 110 as well as the adaptive gain stages 112. In accordance with the presently claimed invention, each of the time delay elements 110 is a fractional delay element and, therefore, imparts to its data

5 signal a time delay of a fraction of the data symbol, and each of the adaptive gain stages 112 is a multiplier that multiplies its respective time-delayed input signal 111 by one of two adaptive coefficient signals 205b, 205c (discussed in more detail below). Additionally, a fat tap adaptation (FTA) stage 200 is included. As discussed in more detail below, this FTA stage 200 provides the adaptive coefficient signals

10 205b, 205c. In accordance with one embodiment, this FTA stage 200 provides these adaptive coefficient signals 205b, 205c in accordance with the error signal 117 and the corresponding time-delayed signal 111a, 111b processed by the related adaptive gain stages 112aa, 112ba. In accordance with another embodiment, the FTA stage 200 also uses the equalization feedback signal 115.

15 It should be understood that, in conformance with the discussion herein, additional pairs of adaptive gain stages 112 can also have corresponding FTA stages 200; however, only one such FTA stage 200 is shown in Figure 2 for purposes of simplified illustration.

By using the adaptive coefficient signals 205b, 205c provided by the FTA

20 stage 200, adaptive gain stages 112aa and 112ba operate as correlated taps since adaptive coefficient signals 205b and 205c are correlated (discussed in more detail below). On the other hand, those among the remaining adaptive gain stages 112ca, ..., 112na-1, 112na that do not use a corresponding FTA stage 200 are independent taps to the extent that their respective adaptive coefficient signals Cca, ..., Cna-1, Can

25 are independent, i.e., uncorrelated.

Referring to Figure 3, one example 200a of the FTA stage 200 (Figure 2) includes multiplier circuits 202a, 202b and control signal generator circuitry implemented as a coefficient signal generator 204a and a timing interpolation parameter signal generator 206a, all interconnected substantially as shown. The

30 adjacent time-delayed feedback signals 111a, 111b are multiplied in their respective multiplier circuits 202a, 202b with the error signal 117. The resulting product signals 203a, 203b are processed by the control signal generator circuits 204a, 206a. As discussed in more detail below, the first control signal generator circuit 204a provides an adaptation control signal 205a to the second control signal generator circuit 206a

which, in return, provides two other adaptation control signals 207a, 207b to the first control signal generator 204a. As a result of processing these input signals 203a, 203b, 207a, 207b, the first control signal generator circuit 204a provides the adaptive coefficient signals c(t)r(t) 205b, c(t)(1-r(t)) 205c, where signal element c(t) is the

5   weighting factor and signal element r(t) is the factor indicative of the degree of correlation between the adjacent time-delayed feedback signals 111a, 111b.

Referring to Figure 4, one example 200aa of the FTA circuit 200a of Figure 3 implements the control signal generators 204a, 206a substantially as shown. In the first control signal generator 204aa, the initial product signals 203a, 203b are further

10 multiplied in further multiplier circuits 212aa, 212ba with the adaptation control signals 207aa, 207ba from the other control signal generator 206aa. An additional constant signal 211 can also be multiplied as part of the product operations, or can be implemented as a constant scaling factor within the multiplier circuits 212aa, 212ba.

The resulting product signal 213aa, 213ba are summed in a signal summing

15 circuit 214. The resulting sum signal 215 is integrated in an integration circuit 216 (e.g., a low pass filter) to produce the first adaptation control signal 205aa. This adaptation control signal 205aa, in addition to being provided to the other control signal generator 206a, is multiplied within further multiplication circuits 218a, 218b with the other adaptation control signals 207aa, 207ba provided by the other control

20 signal generator 206aa. The product signals resulting from these multiplication operations are the adaptive coefficient signals 205ba, 205ca.

In the second control signal generator 206aa, the initial product signals 203a, 203b are differentially summed in a signal summing circuit, where the second product signal 203b is subtracted from the first product signal 203a. The resulting difference

25 signal 223 is multiplied in a multiplier circuit 224a with the adaptation control signal 205aa provided by the first control signal generator 204aa. As with the input multiplier circuits 212aa, 212ba of the first control signal generator 204aa, an additional constant signal 221 can also be used in this multiplication operation, or, alternatively, be implemented as a constant scaling factor within the multiplication

30 circuit 224a operation.

The resulting product signal 225 is integrated by another signal integration circuit 226 (e.g., a low pass filter) to produce one of the adaptation control signals 207aa used by the first control signal generator 204aa.

This adaptation control signal 207aa is further processed by a signal complement circuit 228 in which the input signal 207aa is subtracted from a reference signal having a normalized value, with the resulting difference signal 207ba serving as the other adaptation control signal used by the first control signal generator 204aa.

5   For example, if the value of the incoming signal 207aa were considered to have a normalized signal value range bounded by the values of zero and unity, the signal complement circuit 228 subtracts the incoming signal 207aa from the value of unity to produce the output signal 207ba.

Referring to Figure 5, another embodiment 200b of the FTA circuitry 200

10   (Figure 2) uses alternative implementations 204b, 206b of the control signal generators to process the incoming data signals 111a, 111b, the error signal 117 and the equalization feedback signal 115.

Referring to Figure 6, one implementation 200ab of the FTA circuit 200b of Figure 5 can be implemented substantially as shown. In the first control signal

15   generator 204ba, the time-delayed data signals 111a, 111b and error signal 117 are multiplied in the multiplier circuits 212ab, 212bb (with the multiplication, or scaling, constant 211 included as part of the operation as discussed above) along with the adaptation control signals 207ab, 207bb from the other control signal generator 206ba. The resulting product signals 213ab, 213bb are summed in the summing

20   circuit 214. The resulting sum signal 215 is integrated in the signal integration circuit 216 (e.g., a low pass filter) to produce an adaptation control signal 205ab (which, in this implementation, is used internally and is not provided to the other control signal generator 206ba). This signal 205ab is multiplied in output multiplier circuits 218a, 218b with the adaptation control signals 207ab, 207bb provided by the other control

25   signal generator 206ba to produce the adaptive coefficient signals 205bb, 205cb.

In the second control signal generator 206ba, the equalization feedback signal 115 is differentiated in a signal differentiation circuit 232 (e.g., a high pass filter). The resulting differentiated signal 233 is multiplied in a multiplier circuit 224b with the error signal 117 (with the multiplication, or scaling, constant 221 included as part

30   of the operation as discussed above). The resulting product signal 207ab forms one of the adaptation control signals provided to the first control signal generator 204ba. This signal 207ab is also complemented by the signal complement circuit 228 (as discussed above) to produce the other adaptation control signal 207bb provided to the first control signal generator 204ba.

Referring to Figure 7, an adaptive coefficient signal generator in accordance with another embodiment 300 of the presently claimed invention includes error mixer stages 302, 304, a complement integrating mixer stage 306, an integrating mixer stage 308 and a complement coefficient mixer stage 312, all interconnected substantially as

5   shown. The time-delayed data signals 111a, 111b are received and processed by the error mixer stages 302, 304. Each error mixer stage 302, 304 multiplies these signals 111a, 111b with the error signal 117 in signal multipliers 352, 354. The resulting product signals 353, 355 are summed in a signal combiner 356 and the sum signal 357 is integrated by a signal integration circuit 358 (e.g., a low pass filter).

10   The signals 303, 305 produced by these mixer stages 302, 304 are further processed by the complement integrating mixer stage 306 and integrating mixer stage 308. The complement integrating mixer 306 multiplies signals 303 and 305 in signal multipliers 360, 362 with the signal 309 produced by the integrating mixer stage 308. The resulting product signals 361, 363 are summed in a signal combiner 364. The

15   sum signal 365 is integrated by a signal integration circuit 366 (e.g., a low pass filter).

The integrating mixer stage 308 multiplies signal 303 and signal 305 (which is inverted by a signal inversion circuit 310) in signal multipliers 370, 372 with the signal 307 produced by the complement integrating mixer stage 306. The resulting product signals 371, 373 are summed in a signal combiner 374. The sum signal 375 is

20   integrated by a signal integration circuit 376 (e.g., a low pass filter).

The signals 307, 309 produced by the complement integrating mixer stage 306 and integrating mixer stage 308 are multiplied in the signal multipliers 380, 382 of the complement coefficient mixer stage 312 with the signal 309 produced by the integrating mixer stage 308. The resulting product signals 381, 383 are integrated in

25   respective signal integration circuits 384, 386 (e.g., low pass filters), thereby producing the adaptive coefficient signals 205bc, 205cc.

Referring to Figure 8, an adaptive coefficient signal generator in accordance with another embodiment 240 of the presently claimed invention shares some similarities with the implementation shown in Figure 6. The data signals 111a, 111b

30   are multiplied in multiplier circuits 212ac, 212bc (with a multiplication, or scaling, constant 211 as desired). The resulting product signals 213ac, 213bc are summed in a signal combiner 214a and the sum signal 215a is buffered by a gain stage 214b. The resulting buffered signal 215b is multiplied in a signal multiplier 118 with an integrated signal 245 (discussed in more detail below) to produce the equalization

feedback signal 115a, and is also processed by two signal delay stages 246, 248 (discussed in more detail below).

The buffered signal 215b is processed by the first signal delay stage 246, which compensates for signal delays introduced by the signal slicer 106 (Figure 1),

5   the feedback signal multiplication circuit 118 and the feedback signal summing circuitry 108 (Figure 1) while subtracting out a delay corresponding to that introduced by the signal inversion circuitry 250 and signal differentiation circuit 232a. The delayed signal 247 is inverted in a signal inversion circuit 250. The inverted signal 251 is differentiated in a signal differentiation circuit 232a (e.g., a high pass filter).

10   The differentiated signal 233a is multiplied in a signal multiplier 224c with the error signal 117 (along with a multiplication, or scaling, constant 221 as desired). The resulting product signal 225c is integrated in a signal integration circuit 226a (e.g., a low pass filter) to produce the adaptation control signal 227a for signal multiplier 212bc. This signal 227a is also complemented by a signal complement circuit 228a

15   (as discussed above) to produce the other adaptation control signal 229a for signal multiplier 212ac.

The second signal delay stage 248 compensates for signal delays introduced by the signal slicer 106 (Figure 1), the feedback multiplier 118 and feedback signal summer 108 (Figure 1). The resulting delayed signal 249 is multiplied in a signal

20   multiplier 242 with the error signal 117. The resulting product signal 243 is integrated in a signal integration circuit 244 (e.g., a low pass filter). The integrated signal 245 is multiplied with the buffered signal 215b in the feedback signal multiplier 118 to produce the equalization feedback signal 115a.

Referring to Figure 9, the adaptive coefficient signals as discussed above can

25   be used in an adaptive signal equalizer with fractionally-spaced feedback in a number of ways. As discussed above, the time-delayed data signals 111a, 111b are multiplied in signal multipliers 112aa, 112ba with the adaptive coefficient signals 205b, 205c, with the resulting product signals 113aa, 113ba combined in a signal combiner 114a to produce a signal 115a which may or may not be the final equalization feedback

30   signal (discussed in more detail below). For example, in scenario A, the first adaptation control signal 205b corresponds to a product of a weighting factor c(t) and the correlation factor r(t), while the second adaptation control signal 205c corresponds to a product of the weighting factor c(t) and the complement [1-r(t)] of the correlation factor r(t). The sum signal 115a can be used directly as the final equalization

feedback signal or can be further scaled (e.g., multiplied by a value of unity) in the output multiplier 114b to produce the final equalization feedback signal 115b.

In scenario B, the first adaptation control signal 205b corresponds to a product of a partial weighting factor $c_1(t)$ and the correlation factor $r(t)$, while the second adaptation control signal 205c corresponds to a product of the partial weighting factor $c_1(t)$ and the complement $[1-r(t)]$ of the correlation factor $r(t)$. The sum signal 115a is multiplied in the multiplier 114b by a final weighting factor $c_2(t)$ to produce the final equalization feedback signal 115b.

In scenario C, the first adaptation control signal 205b corresponds to the correlation factor $r(t)$, while the second adaptation control signal 205c corresponds to the complement $[1-r(t)]$ of the correlation factor $r(t)$. The sum signal 115a is multiplied in the output multiplier 114b by the weighting factor $c(t)$ to produce the final equalization feedback signal 115b.

A number of enhancements or modifications may be used to improve the performance over the IFTA with two taps within the fat tap.

Fixed ratio fat tap with Hypothesis testing

In this modification, adaptation of r may not occur in a continuous-time basis. One tap in the fat tap may be set to be at c with LMS adaptation (discrete-time or continuous-time), while the coefficient of the other tap within the fat tap is related to the first tap coefficient as a multiple by a correlation parameter (of the form $\frac{1-r}{r}$ as described above). A discrete set of such hypotheses corresponding to different values of the correlation parameter $\frac{1-r}{r}$ may be assumed. Each hypothesis is tested and the different taps, which may be LMS-adaptable, are adapted and, after convergence, the steady-state mean square error and/or the adapted filter coefficients may be used to decide on the right hypothesis (the right hypothesis may be selected to be the one with minimum MSE and/or acceptable patterns within the tap coefficients).

Multi-tap fat tap with linear interpolation

Multiple taps (more than two) and/or a variable number of taps may be used within a fat tap. A simple but effective approach here is to do multiple stages of linear interpolation, each stage consisting of a linear interpolation between some two points obtained from the earlier stage to give one new point which may be used in the next stage. The multi-tap fat tap will then have more than two parameters to adapt.

As an example, consider three feedback taps within a fat tap with input signals $s(t), s(t-\tau), s(t-2\cdot\tau)$. Then, $s(t-\tau_{r_1}) = r_1 \cdot s(t) + (1-r_1) \cdot s(t-\tau)$ may first be formed as a linear interpolation of $s(t), s(t-\tau)$, and then

$s(t-\tau_{r_2}) = r_2 \cdot s(t-\tau_{r_1}) + (1-r_2) \cdot s(t-2\cdot\tau)$ is expected to be the symbol-spaced

5   feedback signal. The feedback tap coefficients for the fat tap with input signals

$s(t), s(t-\tau), s(t-2\cdot\tau)$ are then $c \cdot r_1 \cdot r_2, c \cdot (1-r_1) \cdot r_2, c \cdot (1-r_2)$. The adaptation updates

of the 3 parameters r_1, r_2, c in the continuous-time domain are as follows:

$$c(t) = \mu_c \cdot \int_0^t e(v) \cdot [r_1 \cdot r_2 \cdot s(v) + (1-r_1) \cdot r_2 \cdot s(v-\tau) + (1-r_2) \cdot s(v-2\cdot\tau)] dv$$

$$r_1(t) = \mu_r \cdot \int_0^t c(v) \cdot r_2(v) \cdot e(v) \cdot [s(v) - s(v-\tau)] dv$$

10

$$r_2(t) = \mu_r \cdot \int_0^t c(v) \cdot e(v) \cdot [r_1 \cdot s(v) + (1-r_1) \cdot s(v-\tau) - s(v-2\cdot\tau)] dv$$

Knowing a priori the signs of c, r_2 the above equations may be simplified.

With an intermediate output of the fat tap defined as

$$f_i(t) = c \cdot r_1 \cdot r_2 s(t) + c \cdot (1-r_1) \cdot r_2 s(t-\tau),$$

and the final output as

15

$$f(t) = f_i(t) + c \cdot (1-r_2) \cdot s(t-2\cdot\tau),$$

then the following simplified update equations result:

$$r_1(t) = \mu_r \cdot \int_0^t e(v) \cdot \frac{df_i(v)}{dv} dv$$

$$r_2(t) = \mu_r \cdot \int_0^t e(v) \cdot \frac{df(v)}{dv} dv$$

Note that $\frac{df_i(v)}{dv}, \frac{df(v)}{dv}$ may easily be implemented by passing the outputs of the fat

20   tap $f_i(t), f(t)$ through the C-R differentiator block, which is a high-pass filter.

Multi-tap fat tap with superlinear interpolation

More general interpolation can also be employed, especially when more than

two taps are included within the fat tap, such as quadratic interpolation. For example,

with three feedback taps within a fat tap and with input signals

25   $s(t), s(t-\tau), s(t-2\cdot\tau)$, the corresponding tap coefficients may be given as

$c \cdot f_0(r), c \cdot f_1(r), c \cdot f_2(r)$ for some appropriately selected functions $f_0(\cdot), f_1(\cdot), f_2(\cdot)$, which in general may also be functions of more than one parameter. The adaptation updates are then given as:

$$c(t) = \mu_c \cdot \int_0^t e(v) \cdot [f_0(r) \cdot s(v) + f_1(r) \cdot s(v - \tau) + f_2(r) \cdot s(v - 2 \cdot \tau)] dv$$

$$\frac{d}{dt} r(t) = c(t) \cdot e(t) \cdot [f_0'(r) \cdot s(t) + f_1'(r) \cdot s(t - \tau) + f_2'(r) \cdot s(t - 2 \cdot \tau)]$$

which may be approximated by the following explicit update equation for $r(t)$:

$$r(t) = \mu_r \cdot \int_0^t c(v) \cdot e(v) \cdot [f_0'(r) \cdot s(v) + f_1'(r) \cdot s(v - \tau) + f_2'(r) \cdot s(v - 2 \cdot \tau)] dv$$

Fat tap with gain offset

To compensate for a residual but unknown gain offset between the taps in a fat tap or to control the linearity range, a fat tap with gain offset may be used. For example, consider two feedback taps within a fat tap with input signals $s(t), s(t - \tau)$. The tap coefficients for these two taps are then respectively $c \cdot r, c \cdot a \cdot (1 - r)$. The adaptation updates for the three parameters (c, a, r) are then given as:

$$c(t) = \mu_c \cdot \int_0^t e(v) \cdot [r \cdot s(v) + a \cdot (1 - r) \cdot s(v - \tau)] dv$$

$$r(t) = \mu_r \cdot \int_0^t c(v) \cdot e(v) \cdot [s(v) - a \cdot s(v - \tau)] dv$$

$$a(t) = \mu_c \cdot \int_0^t c(v) \cdot e(v) \cdot (1 - r) \cdot s(v - \tau) dv$$

Correlated Fat Tap Adaptation (CFTA)

Multiple fat taps may share one or more taps such that each tap could correspond to more than one symbol (e.g., two symbols). It would then be expected that a set of fat taps together emulate multiple symbol-spaced feedback taps. For example, consider three feedback taps with input signals $s(t), s(t - \tau), s(t - 2 \cdot \tau)$ such that these together could correspond to two symbol-spaced feedback taps. The first fat tap which corresponds to the first past symbol consists of the feedback taps with inputs $s(t), s(t - \tau)$, and the second fat tap corresponds to the second past symbol and consists of the feedback taps with inputs $s(t - \tau), s(t - 2 \cdot \tau)$; thus, the fat taps have an

overlapping feedback tap. The feedback tap coefficients may then be expressed as

$$c_1 \cdot r_1, c_1 \cdot (1 - r_1) + c_2 \cdot r_2, c_2 \cdot (1 - r_2) \,.$$

The update equations for c_1, c_2, r_1, r_2 are similarly expressed as follows:

$$c_1(t) = \mu_c \cdot \int_0^t e(v) \cdot [r_1 \cdot s(v) + (1 - r_1) \cdot s(v - \tau)] dv$$

5

$$r_1(t) = \mu_r \cdot \int_0^t c_1(v) \cdot e(v) \cdot [s(v) - s(v - \tau)] dv$$

$$c_2(t) = \mu_c \cdot \int_0^t e(v) \cdot [r_2 \cdot s(v) + (1 - r_2) \cdot s(v - \tau)] dv$$

$$r_2(t) = \mu_r \cdot \int_0^t c_2(v) \cdot e(v) \cdot [s(v) - s(v - \tau)] dv \,.$$

Quasi-LMSE-based Adaptation Schemes for Fat Tap interpolating mixer

Other adaptation techniques for controlling the timing control ratio parameter

10   in the interpolating mixer within the Fat Tap may also be used. One such technique
may include the use of tap coefficients on the feedforward/feedback equalizers which
adapt based on LMSE, in a manner that this approximates LMSE-based adaptation for
the timing control ratio parameter. Thus, if the feedforward tap coefficients within the
Fat Tap are of the form $\{c_i\}_{i=0}^L$, two alternative manners of adapting the timing control

15   ratio are provided below:

$$r = \mu \cdot \int_0^t (\sum_{i=0}^L w_i \cdot c_i) dt \quad \text{or alternatively} \quad r = \mu \cdot \int_0^t (\sum_{i=0}^L \sum_{j=0}^L w_{i,j} \cdot c_i \cdot c_j) dt$$

for appropriately selected adaptation parameter: μ and real number weights $\{w_i\}_{i=0}^L$ or

$\{w_{i,j}\}_{i,j=0}^{i,j=L}$.

Referring to Figure 10, another embodiment 200c of the FTA circuitry 200

20   (Figure 2) uses alternative implementations 204b, 206c of the control signal
generators to process the incoming time-delayed data signals 111a, 111b, the error
signal 117 and adaptive filter coefficient signals 15 (discussed in more detail below)
from the feedforward filter 102a of the equalizer 100 (Figure 1).

Referring to Figure 11, the feedforward filter 102a processes the incoming

25   data signal 101 to produce the equalized signal 109 using a series of signal delay
elements 32a, 32b, ..., 32n, multiplier circuits 34a, 34b, ..., 34n and output summing
circuit 108a in accordance with well-known techniques. Each of the successively

delayed versions 33a, 33b, ..., 33n of the data signal, as well as the incoming data signal 101, is multiplied in one of the multiplication circuits 34a, 34b, ..., 34n with its respective adaptive filter coefficient signal 15a, 15b, ..., 15n (along with a multiplication, or scaling, constant, as desired). The resulting product signals 35a,

5   35b, ..., 35n are summed in the signal summing circuit 108a, with the resulting sum signal forming the equalized signal 109.

Referring to Figure 12, an adaptive coefficients generator 14 processes the incoming data signal 101 and the error signal 117 using series of signal delay elements 42a, 42b, ..., 42n, signal multipliers 44a, 44b, ..., 44n and signal integrators

10   (e.g., low pass filters) 46a, 46b, ..., 46n in accordance with well known techniques. The incoming signal 101 is successively delayed by the signal delay elements 42a, 42b, ..., 42n to produce successively delayed versions 43a, 43b, ..., 43n of the incoming signal 101. Each of these signals 101, 43a, 43b, ..., 43n is multiplied in its respective signal multiplier 44a, 44b, ..., 44n with the error signal 117 (along with a

15   multiplication, or scaling, constant, as desired). The resulting product signals 45a, 45b, ..., 45n are individually integrated in the signal integration circuits 46a, 46b, ..., 46n to produce the individual adaptive filter coefficient signals 15a, 15b, ..., 15n.

Referring to Figure 13, one embodiment 206ca of this alternative second control signal generator in accordance with the presently claimed invention includes a

20   set of signal weighting circuits (e.g., multipliers) 156a, 156b, ..., 156n, a signal combining (e.g., summing) circuit 158 and a signal integration circuit (e.g., low pass filter) 160, interconnected substantially as shown. Each of the adaptive filter coefficient signals 15a, 15b, ..., 15n is weighted (e.g., multiplied) in a respective multiplier 156a, 156b ..., 156n with a corresponding weighted, or scaled, signal 155a,

25   155b, ..., 155n (as well as a multiplication, or scaling, factor μ 161, as desired). The resulting product signals 157a, 157b, ... 157n are combined (e.g., summed) in the signal combiner 158. The combined signal 159 is integrated (e.g., low pass filtered) by the signal integrator 160 to produce the adaptation control signal 207ac r(t). This signal 207ac is also complemented by signal complement circuitry 228 (as discussed

30   above) to produce the other adaptation control signal 207bc [1-r(t)] provided to the first control signal generator 204b.

Referring to Figure 14, another embodiment 206cb of the second control signal generator 206c in accordance with the presently claimed invention includes an alternative implementation 164 of weighting circuitry for weighting the adaptive filter

coefficient signals 15 with corresponding weighted, or scaled, signals 155 (as well as a multiplication, or scaling, factor μ 161, as desired). Such weighting circuitry 164 can be implemented in accordance with well-known techniques using multiple signal weighting circuits (e.g., multipliers) and signal combining (e.g., summing) circuits to

5   perform the prescribed weighting of the respective adaptive filter coefficient signals 15 with the corresponding weighted, or scaled, signals 155 over the appropriate ranges of i and j. As before, the resultant signal 165 is integrated (e.g., low pass filtered) by a signal integrator 160 to produce the adaptation control signal 207ad r(t). This signal 207ad is also complemented by signal complement circuitry 228 (as

10   discussed above) to produce the other adaptation control signal 207bd [1-r(t)] provided to the first control signal generator 204b.

Alternatively, it should be understood that this technique can also be implemented using adaptive coefficient signals from an adaptive feedback filter 104 (Figure 1).

15   Referring to Figure 15, one implementation 200ac of the FTA circuit 200c of Figure 10 can be implemented substantially as shown. Using the adaptation control signals 207a, 207b from the second control signal generator 206c (e.g., Figure 13 or 14), the first control signal generator 204ba operates as discussed above in connection with Figure 6.

20   Yet another technique for adapting the timing control ratio parameter may be using the "eye monitor" test.

Referring to Figures 16A and 16B, expected performance improvement with use of an analog continuous-time feedforward filter in conjunction with "fat tap" adaptation in accordance with the presently claimed invention is as illustrated. Figure

25   16A illustrates the "eye" diagram for the incoming data signal 101 (Figure 11) prior to equalization, while Figure 16B illustrates the "eye" diagram for the output signal 107 of the slicer 106 following equalization in accordance with the presently claimed invention. As shown, the uncompensated waveform of Figure 16A has "eyes" Ea which are substantially closed, thereby producing a high BER corresponding to an

30   eye-opening penalty approaching infinity. In contrast thereto, the compensated waveform of Figure 16B has "eyes" Eb which are substantially open, thereby producing a low BER corresponding to an eye-opening penalty of approximately three decibels.

Referring to Figure 17, an alternative implementation 100a of the DFE circuitry of Figure 1 in accordance with another embodiment of the presently claimed invention includes the feed forward filter 102 and input signal combining (e.g., summing) circuit 108a, the signal slicer 106, the feedback filter 104, and the signal

5   summing circuit 116, plus feedback timing control circuitry 130. As discussed in more detail below, this timing control circuitry 130 controls the feedback signal 115c so as to optimize the output 107 of the signal slicer 106.

In this embodiment 100a, the input signal 103 representing data is differentially summed in the signal combining circuit 108a with the feedback signal

10   115c to produce the pre-slicer signal 109 which is sliced by the signal slicer 106 (e.g., a voltage comparison circuit) to produce the post-slicer signal 107 representing the data of the input signal 103. This post-slicer signal 107 is differentially summed in the signal combiner 116 with the pre-slicer signal 109 to produce a difference signal 117 representing the difference between the post-slicer 107 and pre-slicer 109 signals,

15   and is also referred to as an error signal. Alternatively, the pre-slicer signal 109 can be processed by an adaptive signal latency control circuit 120, with the resulting processed pre-slicer signal 109a being used in place of the original pre-slicer signal 109. A more detailed discussion of this optional processing circuitry 120 can be found in commonly assigned, co-pending U.S. Patent Application No. 10/321,893,

20   filed December 17, 2002, and entitled "Adaptive Signal Latency Control for Communications Systems Signals", the disclosure of which is incorporated herein by reference.

The input data signal 103 is also differentiated by a signal differentiation circuit 132 (e.g., high pass filter) and the resulting differentiated signal 133 is further

25   delayed by a delay circuit 134 which can be implemented in any of a number of well known conventional ways (including as an interpolating mixer, such as that discussed in U.S. Patent Application No. 10/321,893). The resulting differentiated and delayed signal 135 is combined (e.g., mixed or multiplied) in another signal combiner 136 with the difference signal 117. The resulting signal 137 is filtered in a low pass filter

30   circuit (or alternatively a signal integrator) 138 to produce a control signal 139. This control signal 139 controls a timing control circuit 140 (which can be implemented in any of a number of well known conventional ways) that provides a controllable signal delay for the post-slicer signal 107. It is this controllably delayed post-slicer signal

141 which is filtered by the feedback filter circuit 104 to produce the feedback signal 115c.

The feedback filter circuit 104 can be implemented in a conventional manner, such as that depicted in Figure 1. For example, in Figure 17 (using the feedback filter
5   104 of Figure 1 in the circuit of Figure 17), the incoming signal 141 is processed by a tapped delay line in filter 104 with the product signals in filter 104 (corresponding to the product signals in Figure 1) being summed in a signal summing circuit (corresponding to circuit 114 in Figure 1) to produce the feedback signal 115c.

The delay introduced by the delay circuit 134 is selected so as to cause its
10   internal signal delay to equal the sum of signal delays through the input signal combiner 108a, the adaptive signal latency controller 120 (if used) and signal combiner 116 for the pre-slicer signal 109 and post-slicer 107 signal, less any signal delay introduced by the signal differentiation circuit 132. As a result of this delay being introduced by the delay circuit 134, the control signal 139 will have a
15   substantially zero AC signal component.

It should be understood that the order of the signal differentiation circuit 132 and delay circuit 134 can also be reversed, such that the input signal 103 is first delayed by the delay circuit 134 and then differentiated by the signal differentiation circuit 132 to produce the differentiated and delayed signal 135.

20   Referring to Figure 18, a further alternative implementation 100b of the DFE circuitry of Figure 1 in accordance with another embodiment of the presently claimed invention includes the adaptive signal latency control circuit 120 (discussed in more detail, as noted above, in commonly assigned, co-pending U.S. Patent Application No. 10/321,893, the disclosure of which is incorporated herein by reference). In this
25   embodiment 100b, the control signal 139 produced by the low pass filter 138 serves as the interpolation control signal r(t) for the interpolating mixer within the adaptive signal latency control circuit 120 (see U.S. Patent Application No. 10/321,893), while the interpolation control signal 207 produced by the adaptive signal latency control circuit 120 serves as the timing control signal for the timing control circuit 140.

30   Based upon the foregoing discussion, it should be recognized that each of the exemplary embodiments of the presently claimed invention as depicted and discussed herein offer similar advantages without any one of such embodiments necessarily being preferred over the others. As will be readily appreciated by one of ordinary skill in the art, the particular topology of each embodiment may cause one particular

embodiment to be deemed more advantageous for the specific host system or network in which such embodiment is to be implemented (e.g., due to circuit design rules or layout constraints).

5   Various other modifications and alternations in the structure and method of operation of this invention will be apparent to those skilled in the art without departing from the scope and the spirit of the invention. Although the invention has been described in connection with specific preferred embodiments, it should be understood that the invention as claimed should not be unduly limited to such specific embodiments. It is intended that the following claims define the scope of the present

10   invention and that structures and methods within the scope of these claims and their equivalents be covered thereby.